Minutes of the 47th PGC meeting held on May27, 2020 at 02.30 pm
(Meeting was held online over Google Meet)

Following were present:

1. Dr. A.V. Subramanyam- PGC Chairman
2. Dr. Anubha Gupta - DoAA
3. Dr. Pushpendra Singh
4. Dr. Sriram K
5. Dr.SumitDarak
6. Dr. Syamantak Das
7. Dr. Aasim Khan
8. Dr. Ashish Kumar Pandey
9. Dr. Sankha Basu
10. Dr. Tanmoy Chakraborty
11. Dr. Ganesh Bagler
12. Dr. PraveshBiyani
13. Dr. Saket Anand – Special Invitee
14. Dr. Debarka Sengupta – Special Invitee
15. Dr. Arun Balaji Buduru – Special Invitee
16. Mr. K P Singh - Academic In-charge
17. Ms. Sheetu Ahuja - Manager(Academics)
18. Ms. Priti Patel - AM(Academics)
19. Mr. Ashutosh Brahma -AM(Academics)

At the outset, Chair PGC welcomed all the members/special invitees to the meeting. He informed that Prof. Pushpendra is the new PGC member in the capacity of Ph.D. Coordinator of HCD Department. He also informed that confirmation of the minutes of the 46th meeting will be taken up in the next meeting.

1. **To discuss the request for fee waiver by Mr. Ajay Fuloria (offered admission as a sponsored Ph.D. student) under the guidance of Dr Arun Balaji Buduru. PGC has earlier considered the request and was not in favor of giving fee-waiver, the same was communicated to the student and the advisor. Dr Buduru requested to present his view to PGC to re-consider the fee waiver request for the student.**

   Dr Arun Balaji Buduru briefed the PGC about the background of Mr. Ajay Fuloria (a serving personnel in Indian Army) and put up a proposal that in view of the possible collaborations, and to increase organizational connectivity, PGC may consider fee waiver for Sponsored students who are serving personnel in Indian Army/ Navy/ Air Force.
   Chair PGC clarified that PG regulations does not support the concept of fee waiver to sponsored Ph.D. students. He added that the website does mention regarding fee waiver for sponsored Ph.D. students who are working in Academic Institutes but that too is not mandatory.
   PGC also did not find any financial limitations at the candidate's end for paying the full fee.
   After a brief discussion the PGC has decided that the fee waiver cannot be recommended in this case. Further PGC suggested to explore the possibilities to have an MoU with Indian Army with proper fee arrangement.

2. **To discuss regarding the PG diploma program in partnership with IBM. Given the current situation, the proposal is to take the program up online with a substantial reduction in the program fees. The changed program document is attached as Annexure I. It may be noted that there is no change in the program curriculum.**

Dr. Debarka Sengupta briefed the PGC about the 9-months PG diploma program to be run in partnership with IBM. It was initially approved by the PGC to be conducted on IIITD campus. Now in view of the changed circumstances due to COVID 19 pandemic, the following two changes in the initial proposal are put up for consideration.
The two changes are:

1. Mode of conduct of program will be online (exams will be conducted offline for all 3 trimesters) -LMS facility will be used for lectures etc., which the team is currently exploring.
2. The program fee has been reduced to Rs.2.5 Lakh/student (program fee) – He informed that the fee matter is already under process through the Finance Committee.

He also answered the points raised by the members and added that there is no change in the program curriculum.

During the course of discussion, Dr. Debarka also mentioned that IIIT-D Act and statutes enable the institute to grant degree/diploma through Distance mode learning and this program will be governed under this clause. During discussions Manager (Academics) raised a concern about the program fee for other regular program if and when run online. To this it was clarified that reduction of program fee is only for the inaugural batch of 9-months PG Diploma program being launched from 2020 and it should be quoted in that way only.

After a brief discussion, the PGC agreed to the proposed change no. 1 and mentioned that fee matter should approved by FC. The PGC also recommended for approval of the Senate for running online the 9-months PG diploma program in Data Science and Artificial Intelligence in partnership with IBM (attached along with the minutes).

3. **To discuss regarding below points related to M.Tech. internship**

- Internship guidelines related to Non-GATE students
- Internship guidelines for 2019 batch M.Tech. students
- Eligibility CGPA cut-off for M.Tech. Internship interview

Dr Saket Anand (special invitee) briefed the PGC regarding the meeting held with Director, HoD-ECE, DoAA, Chair PGC, M.Tech.(ECE) Coordinator & Placement Coordinator. During the said meeting, placement related statistics and feedback were analysed and it was observed that many of the Masters students are not found well prepared during the internship interviews and hence a need to put CGPA threshold is felt. Dr. Saket added the goal is to motivate and inspire the students to do better in courses.

Some concerns regarding the CGPA cut-off for M.Tech. internship were raised-

- The CGPA requirement for any opportunity (job/internship) should be put from the industry end and not from the Institute. At the least, PGC should primarily address the academic points which are related to course credits and TAship.
- By adding threshold, unnecessary pressure will be built on the student from the first semester itself.
- Do IITs or any other institute put such thresholds?

- It was also noted that having a CGPA cut-off for appearing in the internship or internship+FT may deprive some students of the opportunity while not having it may lead to some offers being null and void (in case min. graduation requirements are not satisfied).

It was noted that none of the IITs allows internships for Masters students, however, there are few other Universities/ institutes who do allow the similar internships/ practices. In view of the same, it was suggested to seek details regarding practices being followed by BITS (through Prof. B. N. Jain).

This item could not be concluded during the meeting and will be taken forward in the upcoming PGC meeting. Though only few members were present towards the end of 2 hour long meeting (designated duration – 1 hr 30 mins.), they conveyed that CGPA cut-off is Industry driven and it would be good to continue that way. Also, this item will be revisited later as and when detailed data is available.

4. **To discuss regarding Honors in M.Tech. program (below are the proposed requirements which are mostly in line with our BTech program).**

M.Tech. students can graduate with Honors degree, requirements for which may be as follows:
1) The students must earn an additional 8 discipline credits
2) The student must have done 16 credits of Thesis
3) At graduation time students must have 8 CGPA (As per the records of last 4-5 years, around 50% students graduate with >8 CGPA)
4) The student must not have any F grade (This is not there in UG program. Since in M.Tech. students have to do less courses, this might be added. Just a suggestion)

Item Deferred.

5. **To consider recommendation of ECE Deptt. for addition of VLSI Specialisation courses:**

ECE Dept has recommended the below changes in VLSI specialization courses:

to remove:

- VLSI Design & Test Flow
- Memory Design

to add:

- VLSI Design Flow
- Digital Hardware Design
- Low Voltage Analog Circuit Design
- Verification and High-Level Synthesis of VLSI Designs
- Memory Design and Testing
- Intelligent Applications Implementation on Heterogeneous Platform
- Introduction to Nanoelectronics

Ph.D.(ECE) Coordinator briefed the PGC regarding the recommendation of ECE Department to update the list of elective courses as above. This was recommended by VLSI group and further approved by HoD-ECE vide email dated 21st May 2020 (Annexure I, attached below).

PGC has approved the above recommendation of the ECE Department.

6. **CB Department has recommended to consider addition of BDS course under eligibility criteria for admission to M.Tech. CB.**

   M.Tech.(CB) coordinator briefed the PGC regarding the present criteria for M.Tech.(CB) admissions. PGC has noted that BDS is a 4 year Degree program and has been recommended by the CB Deptt. to include BDS in the eligibility criteria for admission to M.Tech. CB program. In view of the same the PGC has approved the recommendation of CB Dept to include BDS in the eligibility criteria for the M.Tech. (CB) program.

7. **Thesis Defense/Scholarly Paper Report Submission name :**

   In a recent decision of the PGC and subsequent approval of the Senate, it was decided to grade Thesis/SP/CapP. During the semester, current practice will be followed, where S/X will be awarded will be awarded for multiple credit registration. When the student is expected to complete the min credit, in that particular semester S/he will be registering for the defense or report submission. Following are the proposed name:

   M.Tech. Thesis Viva (16 Credits)
   Scholarly Paper Report (4/8 Credits)
   Capstone Project Report

   Item deferred.

The meeting ended with a vote of thanks to and by the chair.

Annexure I

Priti Patel <priti@iiitd.ac.in>

Fwd: List of electives for VLSI specialization

Ashutosh Brahma <ashutosh@iiitd.ac.in> Thu, May 28, 2020 at 11:37 AM
To: Priti Patel <priti@iiitd.ac.in>

Ashutosh Brahma
Assistant Manager (Academics)

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---------- Forwarded message ---------
From: **Ashutosh Brahma** <ashutosh@iiitd.ac.in>
Date: Thu, May 21, 2020 at 10:32 AM
Subject: Re: List of electives for VLSI specialization
To: HoD ECE <hod-ece@iiitd.ac.in>
Cc: Sneh Saurabh <sneh@iiitd.ac.in>

Thank you for swift response. Here is the final recommendation:

to remove:
VLSI Design & Test Flow
Memory Design

to add:
VLSI Design Flow
Digital Hardware Design
Low Voltage Analog Circuit Design
Verification and High-Level Synthesis of VLSI Designs
Memory Design and Testing
Intelligent Applications Implementation on Heterogeneous Platform
Introduction to Nanoelectronics
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On Thu, May 21, 2020 at 10:30 AM HoD ECE <hod-ece@iiitd.ac.in> wrote:
I agree

On Thu 21 May, 2020, 10:25 AM Sneh Saurabh, <sneh@iiitd.ac.in> wrote:
Yes, please add "Introduction to Nanoelectronics" course also (Please note the complete name of the course).

Regards,
Sneh

On Thu, May 21, 2020 at 10:17 AM Ashutosh Brahma <ashutosh@iiitd.ac.in> wrote:
Hi Shobha Maam and Sneh Sir

I was about to update it after taking it to PGC. In the meanwhile i have received an email from student to consider DHD and **NanoElectronics**, in specialisation course. I can already see DHD in the recommended list. Can you give us a clarity on NanoElectronics? We are having a PGC this week, so we will together put up this and get it updated.

regards
Ashutosh Brahma
Assistant Manager (Academics)

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On Tue, Jan 21, 2020 at 4:04 PM HoD ECE <hod-ece@iiitd.ac.in> wrote:
Ashutosh,
These courses have been approved by a committee of VLSI faculty and not in a departmental FM. Will that approval suffice?
Thanks,
Shobha

On Tue, Jan 21, 2020 at 2:42 PM Sneh Saurabh <sneh@iiitd.ac.in> wrote:
Hi Shobha,

It seems that approved list of electives for specialization needs to go through department FM.

Please add it in the agenda of department FM or approve yourself (I think these bureaucratic approvals can be given at your end also. It has already been discussed in VLSI group).

I am summarizing what needs approval:

Adding the following courses in the list electives for specialization in VLSI and Embedded Systems:
VLSI Design Flow
Digital Hardware Design
Low Voltage Analog Circuit Design
Verification and High-Level Synthesis of VLSI Designs
Memory Design and Testing
Intelligent Applications Implementation on Heterogeneous Platform

Regards,
Sneh

---------- Forwarded message ---------
From: **Ashutosh Brahma** <ashutosh@iiitd.ac.in>
Date: Tue, Jan 21, 2020 at 11:34 AM
Subject: Re: List of electives for VLSI specialization
To: Sneh Saurabh <sneh@iiitd.ac.in>

Sir,

Anyhow i have missed this email. I hope this has been discussed in Departmental FM and recorded as minutes. If not it may be taken to Department FM and send us in the form of minutes. We will put up this in PGC.

regards
Ashutosh Brahma
Assistant Manager (Academics)

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On Tue, Jan 7, 2020 at 2:19 PM Sneh Saurabh <sneh@iiitd.ac.in> wrote:
Dear Ashutosh,

We need to remove: VLSI Design & Test Flow

We need to add:
VLSI Design Flow
Digital Hardware Design

RF Circuit Design (If it already there with the course number ECE321 then it is OK)
Low Voltage Analog Circuit Design
Verification and High-Level Synthesis of VLSI Designs

If I am missing something, please let me know. Please get the webpage also updated. Once done, please let me know, I will inform students.

Regards,
Sneh

On Mon, Aug 26, 2019 at 5:51 PM Ashutosh Brahma <ashutosh@iiitd.ac.in> wrote:

Sir,

this is the link where all the courses are listed (https://iiitd.ac.in/academics/mtech/vlsi) and following are the courses:

Core Courses:
Three courses constitute the core of this stream. These are:

- Digital VLSI Design
- Analog CMOS Circuit Design
- Advanced Embedded Logic

Elective Courses:
The following are the elective courses which are currently being offered in VLSI and Embedded Systems stream.

- SOC Design & Test
- Mixed Signal Design
- Computer Architecture
- Memory Design
- VLSI Design & Test Flow
- RF Circuit Design
- RF Transceiver Design

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On Mon, Aug 26, 2019 at 2:19 PM Sneh Saurabh <sneh@iiitd.ac.in> wrote:

Dear Ashutosh,

Can you please send the current list of electives for VLSI specialization?
Just to make sure that we do not miss anything.

Regards,
Sneh

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